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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/942,835	08/30/2001	John Robertson Tower	SAR 14108	9999

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EXAMINER	
GEBREMARIAM, SAMUEL A	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 06/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/942,835	TOWER ET AL.	
	Examiner	Art Unit	
	Samuel A. Gebremariam	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,7-11,13-18,20,21,31 and 32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,7-11,13-18,20,21,31 and 32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 18 is objected to because of the following informalities: the limitation "single polysilicon" as recited on line 2 of claim 18 appears to be a typographical error. Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1, 11 and 18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The new claimed limitation of an inter-electrode gap in the substrate of the first conductivity type as recited in claim 1 is not clear as to what it means. The inter-electrode gap (210) is formed on the substrate (110) on top of the gate oxide (101) (refer to fig. 4A for example). Therefore it is not clear how one forms an inter-electrode gap in the substrate.

The limitation of a semiconductor region of the first conductivity type, formed in the inter-electrode gap as recited in claims 1 and 11 is not clear as to what it means. The inter-electrode gap is a gap (empty space). It is not clear how one forms a semiconductor region of first conductivity type in an empty region.

The limitation of an "a semiconductor region of the second conductivity type, formed in the inter-electrode gap of the well region" as recited in claim 18 is unclear as

to what it means. There is only one type of inter-electrode (210) that is described in the disclosure. And it is not clear how one forms a semiconductor region of second conductivity type in an empty region.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> **A person shall be entitled to a patent unless –**
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1 and 32 are rejected under 35 U.S.C. 102(b) as being anticipated by Fujii US patent No. 4,952,523.

Regarding claim 1, As best the examiner is able to ascertain the claimed invention Fujii teaches (figs. 8 and 9) a charge coupled device made on a substrate of a first conductivity type (10), the charge coupled device comprising: a dielectric layer (12) overlaying at least a portion of the substrate, and at least two gate electrodes (42, 44) overlaying the dielectric layer, the at least two gate electrodes configured to define at least two charge wells (the n and p regions of the substrate), the at least two gate electrodes being separated by an inter-electrode gap (the gap between 42 and 44) and apparatus for stabilizing the inter-electrode gap, is a semiconductor region (36) of first conductivity type but having a different dopant concentration than region (10), in the inter-electrode gap.

The recitation of "a charge coupled device made according to a standard CMOS process" is not given patentable weight because it is considered a product-by-process

claim. It is the patentability of the claimed product and not of recited process steps, which must be established. Therefore, when the prior art discloses a product, which reasonably appears to be identical with or only slightly different than the product claimed in a product-by process claim, a rejection based on sections 102 or 103 is fair. A product by process claim directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See In re Fessman, 180 USPQ 324,326(CCPA 1974); In re Marosi et al., 218 USPQ 289,292 (Fed. Cir. 1983); and particularly In re Thorpe, 227 USPQ 964,966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a "product by process " claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claim in "product by process" claim or not.

Regarding claim 32, Fujii teaches (fig. 6) substantially the entire claimed structure of claim 1 above including the at least two gate electrodes include polysilicon gate electrodes (column, 11, lines 10-14).

6. Claim 20 is rejected under 35 U.S.C. 102(e) as being anticipated by Savoye US patent No. 6,489,992.

Regarding claim 20, Savoye teaches a back Illuminated Imager (figs. 4A, 4B and 12) comprising: a substrate of a first conductivity type having (col. 15, lines 62-67): a front side and a back side (back side illuminator); photodetector (CCD imager) formed in the front side of the substrate; a well region (420) of a second conductivity type,

opposite to the first conductivity type (n region), formed in the front side of the substrate and separate from the photodetector, the well region and the substrate forming a semiconductor junction (refer to fig. 4B); and at least one diffusion region (400) in the well region of the second conductivity type forming a component of the back illuminated imager; whereby the component of the back illuminated imager is shielded from photocarriers generated in response to photons received at the back side of the substrate by the semiconductor junction (refer to col. 16, lines 6-17).

Regarding claim 21, Savoye teaches substantially the entire claimed structure of claim 20 above including optics (lens) that are configured to focus radiation onto the imager (col. 28, lines 29-37).

The recitation "an electronic camera system" has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 3, 7, 8-11, 13-15, 18 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujii in view of Ohsawa et al. US patent No. 5,210,433.

Regarding claim 3, Fujii teaches (figs. 8 and 9) substantially the entire claimed structure of claim 1 above except explicitly stating that a further dielectric layer formed over the at least two gate electrodes; and a further gate electrode formed overlying the further dielectric layer and positioned over the inter-electrode gap.

Ohsawa teaches forming dielectric layer (44) over at least two gate electrodes (80) and forming a further electrode (82a) overlying the further dielectric layer and positioned over the inter-electrode gap (region between electrodes 80).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to in corporate the further dielectric layer and the further gate electrode taught by Ohsawa in the structure of Fujii in order to control the gap potential.

Regarding claim 7, Fujii teaches substantially the entire claimed structure of claim 1 above including the means for stabilizing the inter-electrode gap includes means for applying respective bias potentials to the at least two gate electrodes, the bias potentials being sufficient to cause fringing fields from the at least two gate electrodes to extend into the inters electrode gap.

Ohsawa teaches (fig. 11) means for controlling gap potential. Therefore the combined structure of Fujii and Ohsawa inherently capable of causing fringing fields as claimed in the gap region. Furthermore since the combined structure of Fujii and Ohsawa teaches two gate electrodes where a bias potential can be applied, the

combined structure is inherently capable of preventing charge carriers from interfering with charge transfer between adjacent electrodes.

Regarding claim 8, Fujii teaches substantially the entire claimed structure of claim 1 above including the charge coupled device further comprises: a well region of a first conductivity type (32), adjacent to the photogate for forming a charge barrier well, the charge barrier well being configured to divert photocarriers into at least the photogate; and a diffusion region of a second conductivity type (12), different from the first conductivity type, the diffusion region being formed inside the charge barrier well and being configured as an anti-blooming drain.

The limitation that the diffusion region being formed inside the charge barrier well and being configured as an anti-blooming drain is not given patentable weight. A recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963).

Regarding claims 9 and 10, Fujii teaches substantially the entire claimed structure of claim 1 above except explicitly stating that a further well region of the first conductivity type, the further well region forming a further charge barrier well; and a

plurality of further diffusion regions of second conductivity type in the further charge barrier well, the plurality of further diffusion regions forming a charge sink.

It is conventional in the art to form more than one well and barrier region in order to form charge coupled device.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form more wells and charge barrier regions in the structure of Fujii in order to form a functional device.

Regarding claim 11, Fujii teaches substantially the entire claimed structure of claim 1 above including a charge coupled device (CCD) array, the array being formed of a plurality of single polysilicon CMOS pixels, each pixel including, a first dielectric layer (12) overlaying the substrate.

The recitation "an optical sensor circuit for receiving photocarriers from a source" has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

Regarding claim 31, Fujii teaches (figs. 8 and 9) substantially the entire claimed structure of claim 11 above including an n-channel region (32). Furthermore the channel region (32) is an n well region.

Regarding claims 13-15, Fujii teaches substantially the entire claimed structure of claims 1, 8-11 above including a diffusion region of a second conductivity type (36), different from the first conductivity type, the diffusion region being formed inside the charge barrier well and being configured as an anti-blooming drain.

Regarding claim 18, Fujii teaches substantially the entire claimed structure of claims 1 and 7 above including that the first and second electrodes are formed of polysilicon (col. 7, lines 54-70) and the first and second gate electrodes being separated by an inter-electrode gap, wherein the combination of the first and second polysilicon gate electrodes, the oxide layer and the well region form a buried channel CCD register (col. 8, lines 32-45) and means for applying respective bias potentials to the at least two gate electrodes, the bias potential being sufficient to cause a fringing field to extend across the inter-electrode gap from at least one of the at least two gate electrodes.

8. Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hieda US patent No. 6,088,057 in view of Fujii.

Regarding claims 16 and 17, Hieda teaches (fig. 1) a single monolithic integrated circuit including CCD imager (2) (fig. 1) and a CMOS analog to digital converter (3) coupled to receive image signals from the CCD optical integration section (fig. 1).

Hieda does not explicitly teach an array of CCD imager.

It is conventional and also taught by Fujii forming an array of CCD imagers as illustrated in figs. 8 and 9.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form an array of CCD imager as taught by Fujii in the structure of Hieda in order to form an imaging device with reduced dark current.

The recitation "a camera system" has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

Response to Arguments

9. Applicant's arguments filed 3/10/05 have been fully considered but they are not persuasive. In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., the subject invention, as defined by claim 1, requires that a semiconductor region of the first conductivity type formed in the inter-electrode gap. As mentioned above it is not clear how one forms a semiconductor region of first conductivity type in an empty region. Refer also to 35 U.S.C. 112 second paragraph rejection. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Therefore the reference of Fujii reads on the claim limitation of a substrate (10) of first

conductive type (p) and a semiconductor region (36) of first conductivity type but having a different dopant concentration than region (10), in the inter-electrode gap as claimed.

With regards to applicant's argument that Fuji fails to teach the dielectric layer overlying at least a portion of the substrate to be a CMOS gate dielectric, made by using standard CMOS process is not given patentable weight because it is considered a product-by-process claim. It is the patentability of the claimed product and not of recited process steps, which must be established. Therefore, when the prior art discloses a product, which reasonably appears to be identical with or only slightly different than the product claimed in a product-by process claim, a rejection based on sections 102 or 103 is fair. A product by process claim directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See In re Fessman, 180 USPQ 324,326(CCPA 1974); In re Marosi et al., 218 USPQ 289,292 (Fed. Cir. 1983); and particularly In re Thorpe, 227 USPQ 964,966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a "product by process " claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claim in "product by process" claim or not.

In response to applicant's argument regarding claim 7, that there is no suggestion to combine the references of Fujii and Ohsawa, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion,

or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case since the combined structure of Fujii and Ohsawa teaches two gate electrodes where a bias potential can be applied, the combined structure is inherently capable of preventing charge carriers from interfering with charge transfer between adjacent electrodes.

In response to applicant's argument that the examiner's conclusion of obviousness with regards to claim 16 and 17 is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

With regards to claims 7, 11 and 18 applicant argues that the combination of Fuji and Ohsawa et al. is improper and a prima facie obviousness rejection requires that the modification of one reference be based on motivation evidenced in the record. In response to the above argument, the fact that applicant has recognized another advantage which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. See *Ex parte Obiaya*, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985).

With regards to claims 20 and 21 applicant argues Savoye fails to teach the claimed limitation as recited in the claims. Clearly stated Savoye teaches a back Illuminated Imager (figs. 4A, 4B and 12) comprising: a substrate of a first conductivity type having (col. 15, lines 62-67): a front side and a back side (back side illuminator); photodetector (CCD imager) formed in the front side of the substrate; a well region (420) of a second conductivity type, opposite to the first conductivity type (n region), formed in the front side of the substrate and separate from the photodetector, the well region and the substrate forming a semiconductor junction (refer to fig. 4B); and at least one diffusion region (400) in the well region of the second conductivity type forming a component of the back illuminated imager; whereby the component of the back illuminated imager is shielded from photocarriers generated in response to photons received at the back side of the substrate by the semiconductor junction (refer to col. 16, lines 6-17).

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel Admassu Gebremariam whose telephone number is 703 305 1913. The examiner can normally be reached on 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Samuel Admassu Gebremariam
May 31, 2005

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